What is claimed is:

1. A system for detecting bit errors within a received bit stream, the system comprising:

a bit stream comparison unit that is adapted to compare a first bit value sequence of the received bit stream to a second bit value sequence associated with a transmitted bit stream to detect a sequence difference between the first and second bit value sequences; and

a multi-source agreement compliant electrical connector, wherein the multi-source agreement compliant electrical connector is adapted to convey the transmitted and received bit streams and is in communication with the bit stream comparison unit, and wherein the multi-source agreement compliant electrical connector is adapted to be directly mechanically and electrically coupled to a multi-source agreement compliant device.

2. The system of claim 1, wherein the bit stream comparison unit and the multi-source agreement compliant electrical connector are integrated on a circuit substrate.

3. The system of claim 2, wherein the circuit substrate is a printed circuit board.

4. The system of claim 1, wherein the multi-source agreement compliant device is an optical transceiver.

5. A system for determining a bit error rate of a device under test, the system comprising:

a bit stream generator adapted to generate a first bit stream to be transmitted to the device under test;

a bit stream comparison unit adapted to compare a second bit stream received from the device under test to the first bit stream;

a processing unit coupled to the bit stream generator and the bit stream comparison unit adapted to determine the bit error rate of the device under test based on the comparison of the second bit stream to the first bit stream; and

an electrical connector including a unitary connector body, wherein the electrical connector is adapted to directly couple to a multi-source agreement compliant connection associated with the device under test.

6. The system of claim 5, further including a display unit coupled to the processing unit, wherein the display unit is adapted to display the bit error rate of the device under test.

7. The system of claim 5, wherein the device under test includes an optical transceiver.

8. The system of claim 5, wherein the processing unit includes a reduced instruction set computer.

9. The system of claim 5, further including a light source that illuminates in response to detection of at least one bit error associated with the second bit stream.

10. A printed circuit assembly for use in detecting a bit error rate, the printed circuit assembly comprising:

a printed circuit board;

a bit stream generation circuit disposed on the printed circuit board;

a bit stream comparison circuit disposed on the printed circuit board and adapted to generate an output for use in detecting the bit error rate; and

a multi-source agreement compliant electrical connector disposed on the printed circuit board and electrically coupled to the bit stream generation circuit and the bit stream comparison circuit.

11. The printed circuit assembly of claim 10, further including a display circuit adapted to provide an output indicative of one of a bit error and the bit error rate.

12. The printed circuit assembly of claim 11, wherein the output indicative of the one of the bit error and the bit error rate is one of a light source and a displayed numeric value.

13. An apparatus for testing a multi-source agreement compliant optical transceiver, comprising:

a printed circuit substrate;

a bit stream generation circuit disposed on the printed circuit substrate;

a bit stream comparison circuit disposed on the printed circuit substrate;

a multi-source agreement compliant electrical connector disposed on the printed circuit substrate and electrically coupled to the bit stream generation circuit and the bit stream comparison circuit; and

a bit error indication circuit disposed on the printed circuit substrate.

14. The apparatus of claim 13, wherein the bit error indication circuit is adapted to illuminate a light source disposed on the printed circuit substrate.

15. The apparatus of claim 13, wherein the bit error indication circuit is adapted to generate a signal that causes a numeric display device to display a bit error rate value associated with the multi-source agreement compliant optical transceiver.

16. A method of testing an optical transceiver, comprising:

directly connecting the optical transceiver to a printed circuit assembly via a multi-source agreement compliant connection;

transmitting a first bit stream from the printed circuit assembly to the optical transceiver via the multi-source agreement compliant connection;

receiving a second bit stream from the optical transceiver at the printed circuit assembly via the multi-source agreement compliant connection;

comparing the first and second bit streams at the printed circuit assembly;

detecting a bit error of the optical transceiver based on the comparison of the first and second bit streams; and

displaying an indication of the detected bit error via a display device.

17. The method of claim 16, further including calculating a bit error rate of the optical transceiver based on the comparison of the first and second bit streams.

18. The method of claim 17, further including displaying the bit error rate via the display device.

19. The method of claim 18, wherein directly connecting the optical transceiver to the printed circuit assembly via the multi-source agreement compliant connection includes attaching the optical transceiver to the printed circuit assembly via a unitary connector mounted to the printed circuit assembly.

20. A method of determining a bit error rate for each of a plurality of MSA compliant optical transceivers, the method comprising:

directly connecting each of the plurality of MSA compliant optical transceivers to a respective one of a plurality of printed circuit assemblies, each of which includes an MSA compliant connection and each of which is adapted to detect bit errors in a bit stream received from its respective one of the plurality of MSA compliant optical transceivers;

placing the plurality of MSA compliant optical transceivers and the plurality of printed circuit assemblies in an environmental test chamber; and

detecting bit errors associated with each of the plurality of MSA compliant optical transceivers while each of the plurality of MSA compliant optical transceivers is under test in the environmental test chamber.

21. The method of claim 20, further including calculating a bit error rate for each of the plurality of MSA compliant optical transceivers.

22. The method of claim 21, further including displaying an indication of one of the detected bit errors and bit error rates via a plurality of display devices, each of which is uniquely associated with one of the plurality of MSA compliant optical transceivers.